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| EXAMINER | |
|---|---|
| RUTLAND WALLIS, MICHAEL | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/817,629 | BIENVENU ET AL. | |
| | Examiner | Art Unit | |
| | Michael Rutland-Wallis | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments filed 6/08/2007 have been fully considered but they are not persuasive.

In response to the *35 USC* § 112 second paragraph rejection Applicant cites Fig. 4 and paragraphs 53-61 reproduced below for clarification. Applicant cites "a first means 88 turns off the switch 81 with a turn-off delay, and a second means 86 turns on the switch 81 with a turn-on delay shorter than the turn-off delay", however as may be seen below the cited language is absent from the disclosure.

> **[53] FIG. 4** shows a preferred embodiment of device ***8*** of **FIG. 3** according to an embodiment of the present invention (autonomous device integrating the turn-off time constant).

**[54]** According to this embodiment, preferably implemented as an integrated circuit, switch ***81*** is an N-channel MOS transistor. The drain of transistor ***81*** is directly connected to a terminal ***84*** of device ***8*** intended to be connected to ground connection terminal ***14*** of circuit ***1*** to be protected. Its source is directly connected to a terminal ***85*** of device ***8*** intended to be directly connected to ground ***32*** (or to the most negative terminal of the power supply). The gate of transistor ***81*** is connected, via a first resistor ***86*** in series with a diode ***87***, to detection input terminal ***83***. The cathode of diode ***87*** is directly connected to the gate of transistor ***81*** while its anode is connected, by resistor ***86***, to terminal ***83***. The gate of transistor ***81*** is further connected to terminal ***84*** by a second resistor ***88***, preferably greater than the value of resistor ***86***.

**[55]** When a positive voltage is present on terminal ***83*** (positive supply voltage), diode ***87*** conducts and transistor ***81*** is on.

**[56]** In the case of a polarity reversal of voltage Vbat, diode ***87*** immediately blocks. Transistor ***81*** however remains on for as long as resistor ***88*** has not discharged its gate capacitance. If the polarity reversal is transient, the transistor gate has no time to discharge. When the transient disturbance disappears, diode ***87*** becomes conductive again and transistor ***81*** is back on. The turning-on of transistor ***81*** is conditioned by the charge of its gate capacitance through resistor ***86***.

**[57]** If the polarity reversal carries on, transistor ***81*** turns off, which prevents the short-circuiting of the power supply.

**[58]** The value of resistor ***88*** is set according to the gate capacitance of transistor ***81*** and to the maximum duration of the transient polarity reversals for which the circuit is not

> desired to be turned off (for example, to have a time constant on the order of one millisecond).
>
> **[59]** Preferably, a zener diode ***89*** connects the gate of transistor ***81*** to terminal ***84***, its anode being connected to terminal ***84***. The function of this diode is to limit the gate-source voltage of transistor ***81*** when said transistor is on to the threshold voltage of diode ***89*** plus the gate-source voltage of transistor ***81***. Also, the diode 89 limits the gate-drain voltage of the transistor 81 to the diode's zener voltage during a transient polarity reversal.
>
> **[60]** In the case of the use of an N-channel MOS transistor as a switch ***81***, it will be ascertained to connect the bulk to the drain to avoid, by a connection of the bulk to the source, the presence of a parasitic diode that would be forward-biased during polarity reversals.
>
> **[61]** The value of resistor ***86*** is, preferably, selected to be as small as possible (for example, at least ten times smaller than that of resistor ***88***. Resistor ***86*** may even be omitted if the voltage on terminal ***83*** does not risk exceeding the avalanche voltage of diode ***89***, resistor ***86*** of which limits its current. Since resistor ***86*** has a value smaller than that of resistor ***88***, the turning-on is faster than the turning-off. This especially enables respecting the required speeds for the starting of circuit ***1*** (or the restarting after a transient disturbance).

It is therefore requested Applicant add a description similar to that present in the Remarks to the disclosure in order to satisfy the requirements set forth in MPEP 2181 [R-5] II. Currently the disclosure fails to satisfy this requirement, and therefore the rejection is maintained.

In response the previous claim objections Applicant's amendments are fully responsive sufficient to obviate the previous objections.

In response to the *35 USC* § 102 rejections made in view of Pechlaner. Applicant contends Pechlaner fails to disclose a device for protecting a circuit against a polarity reversal, the device comprising a controllable switch interposed between a first terminal of a DC power supply and a first terminal of the circuit. In support of this Applicant cites

the location of the controllable switch of Pechlaner is not interposed as claimed. That is the controllable switch of Pechlaner is located between the first power supply terminal and ground or the load, which is connected to ground. Pechlaner is directed to the protecting against the wrong polarity (paragraph 2 page 3) connections for power supplies, logical circuits and power semiconductor switches. Pechlaner describes in beginning on page 6 and in Fig. 1 a protection circuit formed in part with a smart semiconductor switch 5 and MOSFET 3. The smart power circuit is connected to the input of a supply identified as Vbb at connection terminal 1; Applicant similarly points out this connection to the supply in the Remarks (page 6). The smart power circuit in Fig. 1 contains five connections identified as: 1, control input IN, ST, GND and OUT. The connection OUT connects to an inductive load and then to GND. The GND connection connects to reference potential terminal 12 of the logical circuitry (see bottom of page 6). Therefore the smart power switch 5 is interposed between the first power supply terminal 1 of DC power supply and terminals of a circuit such as terminals 2 and 12. Further Applicant alleges the protections from polarity reversals described by Pechlaner does in fact protect a circuit as both of these connections conduct current they constitute a circuit.

Applicant alleges Pechlaner in view of Yamada does not render claim 9 obvious. Applicant cites Pechlaner's delay is simply a measure of time, which is nothing more than a number. Applicant contends a delay is physical part of the circuit. The delay in Applicant's claim refers to a resistance, which is present in the connection from the control circuitry to the switch of Pechlaner, i.e. a physical structure. Applicant cites

Yamada fails to teach where Pechlaner is silent on the inner circuitry of the of the control electronics. Yamada is cited to illustrate the circuitry contained within a control circuit such as that of Pechlaner. The control circuitry of Yamada is configured to protect against reverse current using a switch (5). Yamada also shows example circuitry including a comparator and selected sensing resistors used to give circuit characteristics (col. 5 lines 20-25). It would have been obvious to one of ordinary skill in the art at the time of the invention to use circuitry similar to that shown in Yamada in order to carry out the control of the switch of Pechlaner.

In view of the above the rejections is deemed proper and therefore maintained.

***Claim Rejections - 35 USC § 112***

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has failed to set forth in the disclosure an adequate disclosure showing what is meant by the second means for, in claim 1. Therefore claim 1 fails to comply with 112 2$^{nd}$ paragraph to particularly point out and distinctly claim the invention. See MPEP 2181 [R-5] II.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Pechlaner et al. (DE 199 28 760 A1) see English translation attached to this action.

With respect to claims 1 Pechlaner teaches a device for protecting a circuit against a polarity reversal (Fig. 1) of a connection to a DC power supply (not shown see supply terminals Vbb), comprising: a controllable switch (item 5 smart power switch) interposed on said connection between a first terminal (Vbb) of a first voltage of said DC power supply and a first terminal (see terminal 2) of said circuit; and first means (formed with capacitor item 9 connected to item 6 further see page 5 lines 15-20 to effect the switching of item 3 via controller 4) for turning-off with a delay the switch in the presence of a reverse polarity; and second means (formed by delay associated with the transmit of a control signal from the controller to the switch) for turning on the switch (5) with a delay shorter than the turn-off delay, when the polarity is normal.

With respect to claim 3 Pechlaner teaches the first terminal of the circuit to be protected is a ground connection terminal (item 2 connected to chassis of the system)

With respect to claim 4 Pechlaner teaches the first means comprise a microcontroller (item 4 "controller") having an output controlling, directly or via a selective delay element, said switch

With respect to claim 5 Pechlaner teaches the switch is a MOS transistor with an N channel (see schematic symbol in Fig. 1).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechlaner et al. (DE 199 28 760 A1)

With respect to claim 2 Pechlaner teaches delay is chosen such that an inductive load is switched by the controllable switch (item 5) and not other means (such as item 6) see page 5 lines 15-20. Pechlaner does not teach the delay is chosen based on transient polarity reversal, however the capacitor of Pechlaner would provide a protection from transient reversals via the time constant associated with the capacitor item 9. It would have been obvious to one of ordinary skill in the art at the time of the invention to size the capacitor appropriately to provide a longer or shorter delay based on expected transients from the load or supply in order to insure the load is switched by the controllable switch to prevent damage.

With respect to claim 6 Pechlaner is silent on the circuitry contained within the first means however output terminals of controllers are typically formed with resistive

connections. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a resistor in the connection line from the controller to the switch in order to regulate the voltage drop supplied to protect the switch from damage.

With respect to claim 7 Pechlaner is silent on the use of the first or second resistor Pechlaner teaches the connection of a control diode (item 13) in the controller, however is silent on the nature of the detailed connection of the diode in relation to the control circuitry contained within the controller. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a series of resistors in the connection line from the controller to the switch in order to regulate the voltage drop supplied to protect the switch from damage.

With respect to claim 8 Pechlaner teaches the connection of a control diode (item 13) in the controller, however is silent on the nature of the detailed connection of the diode in relation to the control circuitry contained within the controller. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the zener diode as the control diodes are commonly used as control diodes.

Claims 9-10 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechlaner et al. (DE 199 28 760 A1) in view of Yoshida (U.S. Pat. No. 5,726,505)

With respect to claims 9-10 and 13-20 Pechlaner teaches a circuit (Fig. 1), comprising: a switch (3) operable to conduct a current to a first node of a power supply (connected at terminal Vbb) when the first node has a predetermined polarity relative to a second node of the power supply; and a first delay (formed by delay associated with

the transmit of a control signal from the controller item 4 to the switch item 3) coupled to the switch and operable to disable the switch from conducting current. Pechlaner is silent on teaching the disabling of the switch from the conducting current is preformed at a predetermined time after the polarity reverses in part because a circuitry within the controller is not described or shown in detail. Yoshida teaches system similar protection system (Fig. 2) wherein Yoshida teaches a detection and control circuit (item 6) to operate with delay determined by the component value of the circuitry contained within the circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a predetermined delay if in fact the delay present in Pechlaner is not predetermined in order to allow sufficient time to determine polarity before closing the switch to better protect the load.

With respect to claim 11 Pechlaner teaches a second delay disabling the switch in response to a normal condition of the current (when the removal of power occurs in device of Pechlaner capacitor item 9 provides a delay).

With respect to claim 12 Pechlaner teaches the switch comprises a transistor (see schematic symbol in Fig. 1); and the first delay (4) is operable to discharge the gate capacitance (gate capacitance is inherent to MOSFETs) of the transistor.

## *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MRW

7/7/07

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